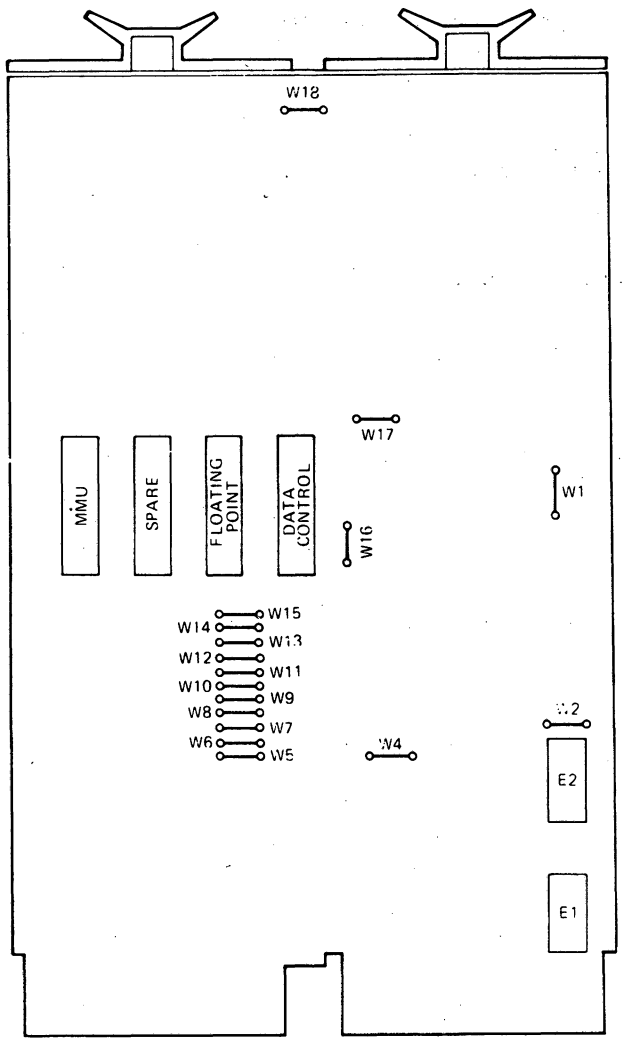
KDF11-AA, AC Configuration Guide (M8186)



R = Jumper Removed
I = Jumper Inserted

1. Power-Up Mode Selection

Mode	Jumpers W6	Jumpers W5	Description
Ø*	R	R	PC at 24 PS at 26
1	R	I	ODT Microcode
2	I	R	PC at Bootstrap. Address determined by jumpers W8-W15.
3	I	I	Microcode boot (not implemented).

*factory configured

2. Bootstrap Address Selection

-used with power-up mode 2.

Jumper*	Function
W8	I = PC at 173000 R = PC determined by W15-W9
W15-W9	Determines high byte of bootstrap address (PC) I - Logic 1 R - Logic Ø

Bootstrap address using jumpers W15-W9 .

15							8	7						Ø
R	R	R	R	R	R	R	X	X	X	X	X	X	X	X
W	W	W	W	W	W	W	0			0			0	
15	14	13	12	11	10	9								

*Factory configured jumpers W8-W15 installed.

3. Event Line Interrupt
jumper W4

I - Disables Event Line Interrupts

*R - Will allow event line interrupts if the PS priority is 5 or less.

*factory configured

4. Misc.

W7 HALT/TRAP

I - With the processor in kernal mode and BPOK H asserted, a HALT instruction will cause the processor to trap to location 10_8.

*R - With the processor in kernal mode and BPOK H asserted, a HALT instruction will force the processor into ODT.

Note: In user mode, a HALT instruction will always cause the processor to trap to location 10_8.

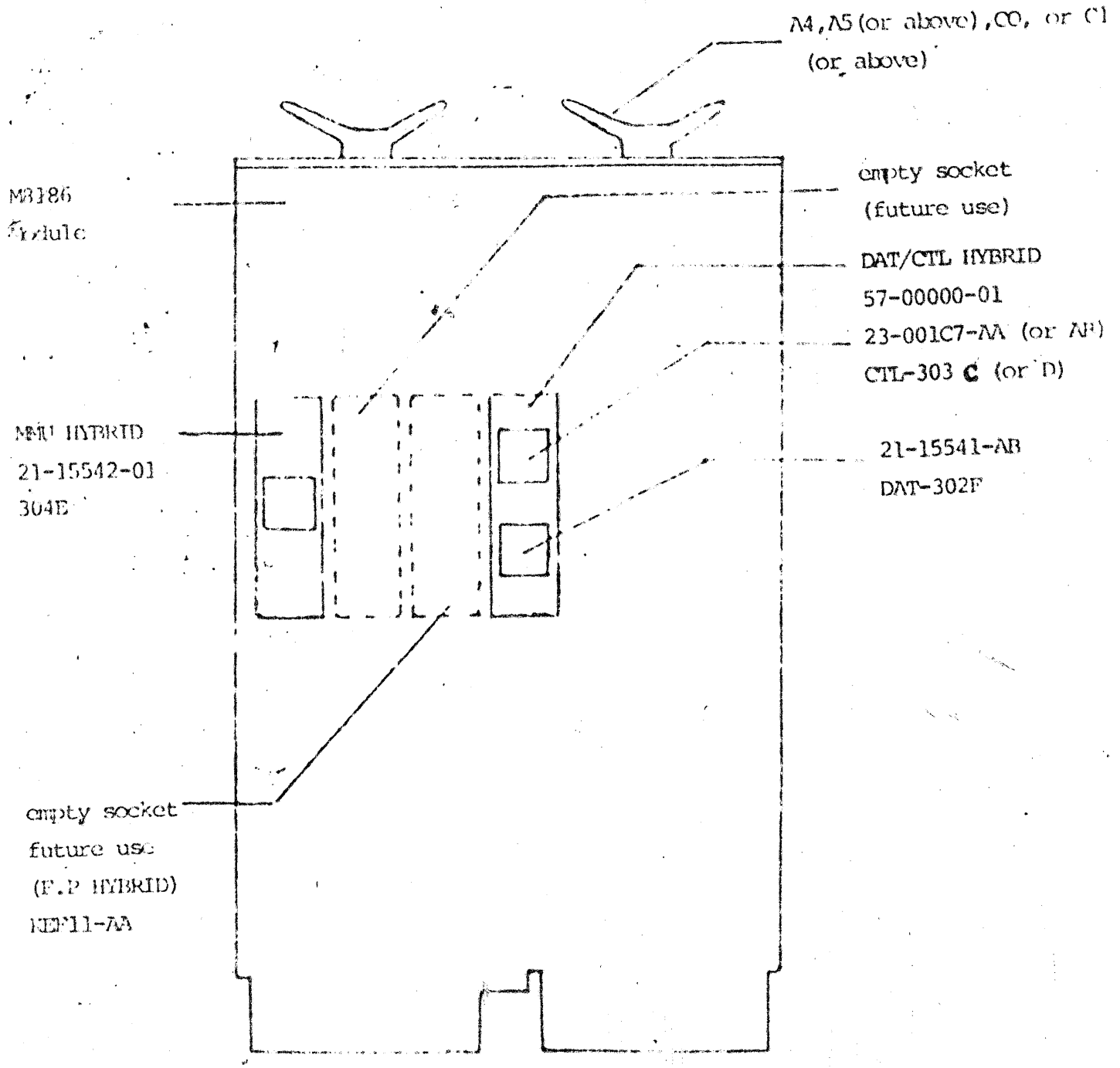
W1 Master Clock Enable

*I - Enable internal clock and should not be removed.

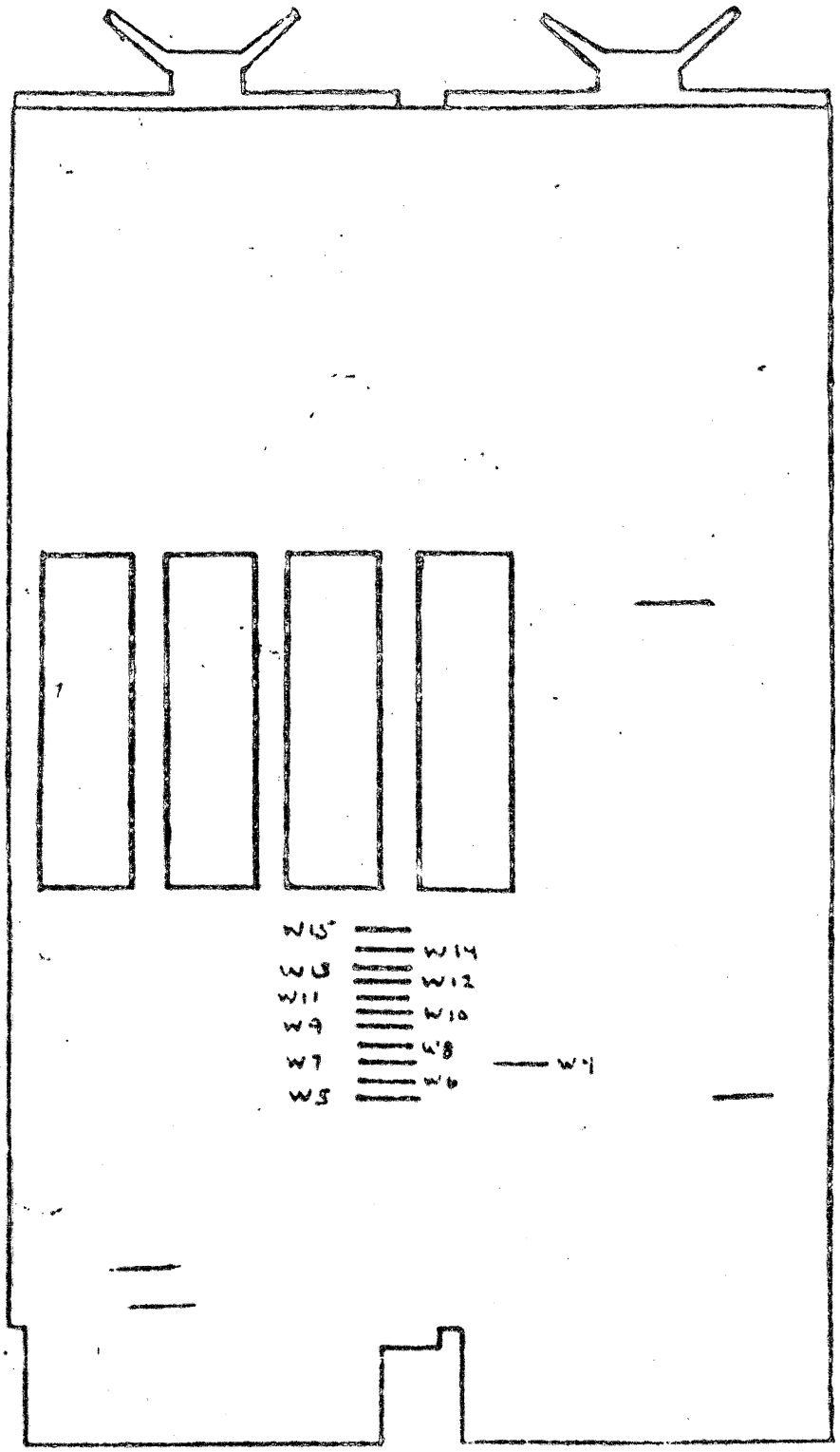
*factory configured

W2, W16, W17, W18 are DEC reserved and should not be altered.

GUIDE TO FLOATING POINT COMPATIBLE MODULES



KDF11-AA SHOWING CHIP SET FOR FLOATING POINT COMPATIBILITY



KDF-11 rev. C and later